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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,892	02/26/2002	Pradeep Trivedi	03226/166001 (P7131)	2795

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,892	TRIVEDI ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-16,24-28 and 36-40* is/are rejected.

7)☒ Claim(s) *17-23,29-35 and 41-47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated December 12, 2005.

2. Claims 1-10 and 12-47 are presented for examination. Applicant has canceled claim 11.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6, 10, 12, 14-16, 24, 26-28, 36, 38-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Parry et al., US Patent 6680636, hereinafter Parry.

5. In re claim 1, Parry discloses an integrated circuit [clock edge placement circuit], comprising [col.3, l.46 – col.4, l.8]:

- A clock source [external] that outputs a clock signal, wherein the clock signal propagates down a first path [path leading to delay line].
- A first biasable delay driver [delay line biased accordingly to ensure synchronous sampling] that inputs the clock signal at a point on the first path [delay line receives the clock signal].
- Wherein the first biasable delay driver is selectively siz93ed [propagation delay] based on a delay of the clock signal from the clock source to the point on the first path [delay at

input point to delay line affects biasing of propagation delay to ultimately ensure synchronous sampling].

6. As to claim 2, Parry discloses, the first biasable delay driver comprising: a first element [delay line] that inputs the clock signal and outputs a modulated clock signal [601 modulates] and a second element [output line] that inputs the modulated clock signal and outputs a delay biased clock signal, wherein a size of the first element is variable [via taps] [col.12, l.49 – col.13, l.29].

7. As to claim 3, Parry discloses, wherein the second element has a fixed size [output line has fixed characteristic] [col.12, l.49 – col.13, l.29].

8. As to claim 4, Parry discloses, wherein the clock signal propagates down a second path, the integrated circuit further comprising: a second biasable delay driver that inputs the clock signal at a point on the second path, wherein the second biasable delay driver is selectively sized based on a delay of the clock signal from the clock source to the point on the second path [col.2, ll.26-41; col.3, l.46 – col.4, l.8; clocks distributed to multiple chips with separate paths requiring same synchronous biasing].

9. As to claim 6, Parry discloses, wherein a load on the first path and a load on the second path is unbalanced [col.2, ll.26-64; fabrication process variation causes load imbalance among paths through different circuits].

10. As to claims 10, 14, 26, 38, Parry discloses, wherein the clock source is a clock header [col.3, l.46 – col.4, l.8; external clock source distributed].

11. In re claim 12, Parry discloses each and every limitation as discussed above in reference to claim 1. Parry discloses the integrated circuit; therefore, Parry discloses the method of operating the integrated circuit.

12. As to claims 15, 27, 39, Parry discloses, wherein selectively sizing the first biasable delay driver comprises: determining whether the first delay is less than a minimum delay; if the first delay is less than a minimum delay, decreasing a size [via taps] of the first biasable delay driver [col.8, l.54 – col.9, l.25].

13. As to claim 16, 28, 40, Parry discloses, wherein selectively sizing the first biasable delay driver further comprises: determining whether the first delay is greater than a maximum delay; if the first delay is greater than a maximum delay, increasing the size of the first biasable delay driver [col.8, l.54 – col.9, l.25].

14. In re claim 24, Parry discloses each and every limitation as discussed above in reference to claim 1. Parry discloses a computer system [fig.20] comprising a processor, a memory, and instructions, residing in the memory and executable by the processor [inherently, a computer system comprises of a processor, a memory, and instructions, all in the broadest interpretation, in order to be functional].

15. In re claim 36, Parry discloses each and every limitation as discussed above in reference to claim 12. Parry discloses the method; therefore, Parry discloses a computer-readable medium having recorded therein instructions executable by processing for executing the method.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 5, 7-9, 13, 25, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parry as applied to claims 1, 4 above.

18. As to claims 5, 9, 13, 25, 37, Parry discloses each and every limitation as discussed above in reference to claims 1 and 4. Parry did not disclose explicitly that the first and second paths have a capacitive component. Examiner has taken Official Notice that it is very well known in the art to have logical elements [col.2, ll.42-64] that contains a resistive component [inherent in all digital circuitries] and a capacitive component [to store energy or states], in order to provide an operable device.

19. As to claim 6, Parry discloses each and every limitation as discussed above in reference to claim 4. Parry did not disclose explicitly that a load on the first path and a load on the second path is unbalanced. Examiner has taken Official Notice that it is very well known in the art the fabrication process variations [col.2, ll.26-64] can cause a load on the first path and a load on the second path to be unbalanced, which is why Parry is concerned with the problem of synchronous sampling among different paths [abstract].

20. As to claim 7, Parry discloses each and every limitation as discussed above in reference to claim 4. Parry did not disclose explicitly that an RC delay of the first path is not equal to an RC delay of the second path. Examiner has taken Official Notice that it is very well known in the art the fabrication process variations [col.2, ll.26-64] can cause an RC delay of the first path to be not equal to an RC delay of the second path, which is why Parry is concerned with the problem of synchronous sampling among different paths [abstract].

21. As to claim 8, Parry discloses each and every limitation as discussed above in reference to claim 4. Parry did not disclose explicitly that a length of the first path is not equal to a length of the second path. Examiner has taken Official Notice that it is very well known in the art the fabrication process variations [col.2, ll.26-64] can cause a length of the first path to be not equal to a length of the second path, which is why Parry is concerned with the problem of synchronous sampling among different paths [abstract].

Allowable Subject Matter

22. Claims 17-23, 29-35, 41-47 are objected to as being dependent upon a rejected base claim, but would be allowable, as previously indicated, if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

23. All rejections of claim limitations as filed prior to Amendment dated December 12, 2005 not argued in entirety or substantively in response filed as said Amendment have been conceded by Applicant and the rejections are maintained from henceforth. Any arguments hereinafter related to said rejections of claim limitations will be considered untimely.

24. Applicant's arguments filed December 12, 2005 have been fully considered but they are not persuasive. Applicant alleges that Parry fails to disclose "sizing a biasable driver dependent on a delay of a clock signal from a clock source to an input of the biasable driver". Examiner disagrees and submits that Parry does disclose selectively sizing a biasable delay [propagation delay] based on a delay of the clock signal from the clock source to the input of the biasable driver to ultimately ensure synchronous sampling as evidenced by Applicant's concession on pp. 13-14 of Remarks dated December 12, 2005 [particularly, "Parry discloses a clock edge

placement circuit that has a delay line that adds propagation delay to a clock signal at an input of the clock edge placement circuit... to ensure that an edge of the clock signal is placed such it causes optimal sampling by external logic elements"]. Accordingly, Applicant's arguments are deemed not persuasive and the rejections are respectfully maintained.

Conclusion

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Tse Chen
February 3, 2006